AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of executing an instruction comprising:

receiving residual data of a first image and decoded pixels of a second image;

zero-extending a plurality of unsigned data operands of an 8-bit precision of the decoded pixels using one or more qualifiers to determine whether ~~the upper~~ upper or lower unsigned data operands are operated on to produce a plurality of unpaeked data operands;

adding a plurality of signed data operands of a 16-bit precision of the residual data to the plurality of unpacked data operands producing a plurality of signed results, wherein the 16-bit precision is greater than the 8-bit precision;

saturating the plurality of signed results producing a plurality of unsigned results, the unsigned results having the 8-bit precision which is less than the 16-bit precision.

2. (Original) The method as recited in Claim 1, wherein the residual data comprises data results from an inverse diserete cosine transform (DCT) operation and the second image comprises a previously decoded video frame.

3. (Original) The method as recited in Claim 1, wherein the second image is an earlier decoded block from a same video frame as the first image.

4. (Original) The method as recited in Claim 1, wherein the zero-extending, the adding and the saturating are part of a video estimation funetion.

5. (Original) The method as recited in Claim 1, wherein the zero-extending, the adding and the saturating are part of a video compensation function.

6. (Cancelled)

7. (Cancelled)

8. (Original) The method as recited in Claim 1, wherein the method is performed utilizing Single-Instruction/Multiple-Data (SIMD) circuitry.

9-13 (Cancelled)

14. (Currently Amended) An apparatus comprising:

a first plurality of multiplexers, each multiplexer of the first plurality of multiplexers operative to select one of a plurality of unsigned decoded pixels of a first precision and zero-extend the unsigned decoded pixels using one or more qualifiers to determine whether ~~the upper~~ upper or lower unsigned data operands are operated on, the first plurality of multiplexers operative to produce a plurality of unpacked operands;

a plurality of adders, each adder of the plurality of adders operative to add a signed residual data operand of a second precision that is greater than the first precision to one of the plurality of unpacked operands, the plurality of adders operative to produce a plurality of sums,

a plurality of saturation units operative to produce a plurality of unsigned result pixels from the plurality of sums, the unsigned result pixels having the first precision.

15. (Original) The apparatus as recited in Claim 14, further comprising:

a second plurality of multiplexers operative to select between the plurality of unsigned result pixels and zeroes.

16. (Original) The apparatus as recited in Claim 14, wherein the plurality of adders comprises four 16-bit adders.

17. (Original) The apparatus as recited in Claim 14, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction.

18. (Original) The apparatus as recited in Claim 14, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

19. (Original) The apparatus as recited in Claim 14, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

20. (Original) The apparatus as recited in Claim 14, wherein the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units form a Single-Instruction/Multiple-Data (SIMD) instruction execution circuit.

21. (Original) The apparatus as recited in Claim 14, wherein the signed residual data operand comprises data results from an inverse discrete cosine transform (DCT) operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.

22. (Original) The apparatus as recited in Claim 21, wherein the apparatus is utilized by a video compensation function.

23. (Currently Amended) An apparatus comprising:

a coprocessor interface unit to identify an instruction for a mixed-mode operation, a first source having a plurality of signed residual data operands of a first precision and a second source having a

plurality of unsigned decoded pixels of a second precision, the second precision less than the first precision;

an execution unit to perform the mixed-mode operation on the plurality of signed residual data operands and the plurality of unsigned decoded pixels; and

a register to store a result having a plurality of unsigned result pixels of the second precision;

wherein the execution unit comprises:

a first plurality of multiplexers, each multiplexer of the first plurality of multiplexers operative to select one of the plurality of unsigned decoded pixels and zero-extend the unsigned decoded pixels using one or more qualifiers to determine whether ~~the upper~~ upper or lower unsigned data operands are operated on, the first plurality of multiplexers operative to produce a plurality of unpacked operands;

a plurality of adders, each adder of the plurality of adders operative to add one of the plurality of signed residual data operands and one of the plurality of unpacked operands, the plurality of adders operative to produce a plurality of signed sums, and

a plurality of saturation units operative to produce a plurality of unsigned result pixels from the plurality of signed sums.

24. (Original) The apparatus as recited in Claim 23, the execution unit further comprising:

a second plurality of multiplexers operative to select between the plurality of unsigned result pixels and zeroes.

25. (Original) The apparatus as recited in Claim 23, wherein the plurality of adders comprises four 16-bit adders.

26. (Original) The apparatus as recited in Claim 23, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction.

27. (Original) The apparatus as recited in Claim 23, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

28. (Original) The apparatus as recited in Claim 23, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

29. (Original) The apparatus as recited in Claim 23, wherein the signed residual data operands comprise data results from an inverse discrete cosine transform (DCT) operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.

30. (Currently Amended) A data processing system comprising:

an addressable memory to store an instruction for a mixed-mode operation;

a processing core coupled to the addressable memory, the processor core comprising:

an execution core to access the instruction;

a first source register to store a plurality of signed residual data operands of a first precision;

a second source register to store a plurality of unsigned decoded pixels of a second precision that is less than the first precision;

a destination register to store a plurality of unsigned result pixels of the second precision;

a wireless interface to receive an encoded bit stream; and

an I/O system and decoder to provide the plurality of signed residual data operands to the first source register from the encoded bit stream;

wherein the execution core comprises:

a first plurality of multiplexers, each multiplexer of the first plurality of multiplexers operative to select one of the plurality of unsigned decoded pixels and zero-extend the unsigned decoded pixels using one or more qualifiers to determine whether ~~the upper~~ upper or lower unsigned data operands are operated on, the first plurality of multiplexers operative to produce a plurality of unpacked operands;

a plurality of adders, each adder of the plurality of adders operative to add a signed residual data operand to one of the unpacked operands, the plurality of adders operative to produce a plurality of sums, and

a plurality of saturation units operative to produce a plurality of unsigned result pixels.

31. (Original) The data processing system as recited in Claim 30, wherein the plurality of adders comprises four 16-bit adders.

32. (Original) The data processing system as recited in Claim 30, wherein the I/O system and decoder comprise an inverse discrete cosine transform function.

33. (Original) The data processing system as recited in Claim 30, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction.

34. (Original) The data processing system as recited in Claim 30, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

35. (Original) The data processing system as recited in Claim 30, wherein configuration of the first multiplexer, the adders, and the saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

36. (Original) The data processing system as recited in Claim 30, wherein the signed residual data operands comprise data results from an inverse discrete cosine transform (DCT) operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.

37. (New) An apparatus comprising:

a plurality of registers; and

an execution core coupled with the plurality of registers, the execution core to receive an instruction, the instruction indicating a first source register of the plurality of registers and a second source register of the plurality of registers, the first source register to store a first plurality of signed operands of a first precision, the second source register to store a second plurality of unsigned operands of a second precision, the first precision greater than the second precision, and the first plurality less than the second plurality, the execution unit to execute the instruction and to store result operands in a destination register, the result operands being unsigned operands of the second precision that each represent a sum of corresponding operands from the first and second pluralities of operands.

38. (New) The apparatus of claim 37, wherein the result operands have a precision of 8-bits, and wherein the first precision is 16-bits.

39. (New) The apparatus of claim 37, wherein the execution unit is to saturate the result operands to the second precision.

40. (New) The apparatus of claim 37, wherein the results operands each represent a sum of an operand from the first plurality of operands with a corresponding operand from the second plurality

of operands, wherein the corresponding operands from the second plurality of operands consist of operands from one of a most significant half and a least significant half of the second source register.

41. (New) The apparatus of claim 37, wherein the first plurality of operands comprises four operands, and wherein the second plurality of operands comprises eight operands.

42. (New) The apparatus of claim 37, wherein the results in the destination register include four operands.